Claims

1. A method for forming a contact of a semiconductor device, the contact being positioned on a substrate, the substrate having a bit-line contact area and a gate contact area, the method comprising the steps of:

   forming an opening on the gate contact area;

   depositing a dielectric layer on the bit-line contact area and the opening;

   coating a photoresist to define a bit-line contact opening on the bit-line contact area and a gate contact opening on the gate contact area;

   etching the dielectric layer while using the photoresist as a mask to form the bit-line contact opening and the gate contact opening;

   removing the photoresist; and

   forming a conductive layer on the bit-line contact opening and the gate contact opening.

2. The method of claim 1, wherein the depositing step further comprises:

   depositing a borophospho-silicate glass (BPSG) layer;

   annealing the borophospho-silicate glass layer; and

   depositing a tetraethyl orthosilicate (TEOS) layer.

3. The method of claim 2, wherein a deposition depth of the borophospho-silicate glass layer on the bit-line contact area after annealing is 2400~2500Å.

4. The method of claim 2, wherein a deposition depth of the tetraethyl orthosilicate layer is 2600~4500 Å.

5. The method of claim 2, wherein a temperature for annealing the borophospho-silicate glass layer is 850~950℃.

6. The method of claim 1, further comprising forming a polysilicon layer as a hard mask between the depositing step and the coating step.

7. A method for forming a contact of a semiconductor device, the contact being positioned on a substrate, the substrate having a bit-line contact area and a gate contact area, the method comprising the steps of:

forming an opening on the gate contact area;

depositing a borophospho-silicate glass (BPSG) layer on the bit-line contact area and the opening;

annealing the borophospho-silicate glass layer;

depositing a tetraethyl orthosilicate (TEOS) layer;

coating a photoresist to define a bit-line contact opening on the bit-line contact area and a gate contact opening on the gate contact area;

etching the borophospho-silicate glass layer and the tetraethyl orthosilicate layer while using the photoresist as a mask to form the bit-line contact opening and the gate contact opening;

removing the photoresist; and

forming a conductive layer on the bit-line contact opening and the gate contact opening.

8. The method of claim 7, wherein a deposition depth of the borophospho-silicate glass layer on the bit-line contact area after annealing is 2400~2500Å.

9. The method of claim 7, wherein a deposition depth of the tetraethyl orthosilicate layer is 2600~4500 Å.

10. The method of claim 7, wherein a temperature for annealing the borophospho-silicate glass layer is 850~950℃.

11. The method of claim 7, further comprising forming a polysilicon layer as a hard mask between the step of depositing a tetraethyl orthosilicate layer and the coating step.

12. A method for forming a contact of a semiconductor device, the contact being

positioned on a substrate, the substrate having a bit-line contact area and a gate contact area, the method comprising the steps of:

forming an opening on the gate contact area;

depositing a borophospho-silicate glass (BPSG) layer on the bit-line contact area and the opening;

annealing the borophospho-silicate glass layer under a temperature of 850~950℃;

depositing a tetraethyl orthosilicate (TEOS) layer of a depth of 2600~4500 Å;

coating a photoresist to define a bit-line contact opening on the bit-line contact area and a gate contact opening on the gate contact area;

etching the borophospho-silicate glass layer and the tetraethyl orthosilicate layer while using the photoresist as a mask to form the bit-line contact opening and the gate contact opening;

removing the photoresist; and

forming a conductive layer on the bit-line contact opening and the gate contact opening.

13. The method of claim 12, wherein a deposition depth of the borophospho-silicate glass layer on the bit-line contact area after annealing is 2400~2500Å.

14. The method of claim 12, further comprising forming a polysilicon layer as a hard mask between the step of depositing a tetraethyl orthosilicate layer and the coating step.